Adaptation of the Hartree-Fock method in GAMESS (US) to Intel Xeon Phi architecture

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Hartree-Fock (HF) approach is one of the basic *ab initio* methods in quantum chemistry. The idea of this method is iterative solution of Hartree-Fock-Roothaane equation. Each iteration comprises two major steps – construction and subsequent diagonalization of the Fock matrix. In direct HF method the computational cost of the Fock matrix construction is dominated by the calculation of six-dimensional integrals corresponding to the Coulomb repulsion of electrons (electron repulsion integrals, ERI). This step has theoretical $O(N^4)$ computational complexity, where N is a number of basis functions used to characterize the system. However, many of these integrals are small enough and may be neglected thereby reducing the overall complexity of this step to $O(N^{2\div3})$, especially for large and sparse systems. In that case Fock matrix diagonalization ($O(N^3)$) dominates performance of the Hartree-Fock method. However, in most practically important cases the speed of Hatree-Fock method depends solely on the speed of Fock matrix construction and is usually of supercomputer scale. We therefore targeted the Fock matrix two-electron contribution code to demonstrate the applicability of the Intel MIC platform to classical quantum chemistry problems.

In this study we implemented a massively parallel version of the direct Hartree-Fock method in GAMESS (US). GAMESS (US) is one of the oldest and most popular open-source quantum chemical software packages. While used by thousands of research groups in hundreds of compute centers nowadays, many computationally intensive parts of GAMESS (US) code have been written in 70-ies and 80-ies without any consideration for the modern manycore and vectorized type of CPUs. Therefore migrating of GAMESS (US) code to novel types of CPU architectures is of great importance. Current work demonstrates the applicability of Xeon Phi coprocessors for the quantum chemistry problems. We obtained a good scalability of the current implementation on Xeon Phi cores, as well as with multiple Xeon Phi chips running in native mode (OpenMP+MPI parallelization). Future work includes more thorough performance characterization and additional vectorization of ERI calculation.

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